REMARKS

The Examiner's Action mailed on December 12, 2005, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for a Three-month Extension of Time, extending the period for response to June 12, 2006.

In this Amendment, Applicant has amended independent claims 1 and 28. Claims 1 and 28 are the independent claims, and claims 1-31 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner's Action has provisionally rejected independent claims 1 and 28, and various dependent claims, on the ground of non-statutory obviousness-type double patenting. In response, attached to this Amendment is a Terminal Disclaimer, thus rendering this provisional rejection moot.

The Examiner has rejected claims 1-22 as being obvious over *Norman et al.* (USP 5,681,756) in view of *Yamazaki et al.* (US 2002/0070382). It is submitted that these claims are *prima facie* patentably distinguishable over the cited combination of references for at least the following reasons.

Applicant's independent claim 1 is directed to a combined semiconductor apparatus that includes, *inter alia*, a first thin semiconductor film comprised of a first material, which includes at least one semiconductor device, and a second thin

semiconductor film comprised of a second material that is different from the first material, and which includes an integrated circuit and a first terminal. A first individual interconnecting line is provided which electrically connects the semiconductor device and the first thin semiconductor film to the first terminal and the second thin semiconductor film.

Because Applicant's claimed first and second semiconductor thin films are formed of different materials, they can be formed in different processes. Therefore, the manufacturing of the first thin semiconductor film can be made without influencing the manufacturing of the second thin semiconductor film, and the manufacturing of the second thin semiconductor film can be performed without influencing the manufacturing of the first thin semiconductor film. Moreover, the present invention aims to obtain a combined semiconductor apparatus comprising a high-performance semiconductor device (a first thin semiconductor film) and an integrated circuit (a second thin semiconductor film) electrically connected to the semiconductor device, wherein the semiconductor device and the integrated circuit are disposed on a substrate so as to be unified. Therefore, the present invention can achieve space-savings and low assembly costs.

Further, in the present application, a semiconductor device, such as an LED, can be made of a material appropriate for an LED, such as A1GaA5 or A1GaN, and can be manufactured using a dedicated semiconductor

manufacturing process. Therefore, a semiconductor device with a higher luminous intensity and reduced luminous variations can be obtained.

Furthermore, in the present application, an integrated circuit, which can be an electrical circuit connected to the semiconductor device, may be made of another material and by another manufacturing process, wherein the other material and the other manufacturing process of the integrated circuit are different from the material and the manufacturing process of the semiconductor device. Therefore, an integrated circuit with high reliability and high performance can be obtained. Other advantages of the claimed invention are discussed in detail in Applicant's specification, and are neither disclosed nor suggested by the cited references.

Norman et al. is directed to a method of making an integrated multi-color organic LED array. This reference discloses providing a substrate 12, and a metal or heavily doped layer 13 on top of the substrate 12. This reference further discloses that a FET 50 can be formed within the substrate 12 and in contact with layer 13. The Examiner's Action has equated the FET 50 as being a second thin semiconductor film, as recited by Applicant's independent claim 1. However, and as noted above, this FET 50 is not disposed on the substrate, as would be required by Applicant's claim 1, but is instead formed within the substrate 12. Moreover, this FET 50 requires that a high purity semiconductor substrate be used, such as silicon single crystalline substrate, and amorphous silicon substrate,

or a poly-silicon substrate, thereby increasing the cost of the device. In contrast, since Applicant's claimed semiconductor thin semiconductor film is disposed on the substrate, rather than within the substrate, Applicant's claimed invention does not require the high-cost, high-purity semiconductor substrate as would be required by *Norman et al.*

The Examiner's Action also relies on the teaching of *Yamazaki et al.* *Yamazaki et al.* disclose that a wiring layer or a wiring line is used to connect one transistor circuit and another transistor circuit, both of which are disposed on the same surface. This reference discloses a driver circuit 201 and a pixel portion 205 which are manufactured and patterned at the same time. However, and similar to the deficiencies noted above with respect to *Norman et al.*, this reference does not disclose or suggest a first thin semiconductor film which includes a semiconductor device, and a second thin semiconductor film which includes an integrated circuit, both of which are formed on the same surface, and which are comprised of different materials. That is, this reference does not disclose or suggest that an element, other than another transistor circuit, can be disposed on the same surface as the first transistor circuit. Thus, there is no disclosure or suggestion of connecting a transistor circuit and a light-emitting element or a display element, both of which are disposed on the same surface.

Moreover, this reference discloses a transistor (which is shown in Figure 3b as a component located below the orientation film 301, for driving a liquid crystal

display (which is the liquid crystal material 308 shown in Figure 6)). The liquid crystal display is separate from the transistor, but is not formed as a semiconductor thin film, nor is it formed on the same surface of the substrate as the semiconductor thin film.

Moreover, it is respectfully submitted that there would have been no motivation to one skilled in the art to replace a second semiconductor thin film, as disclosed by *Norman et al.*, with a transistor, as disclosed by *Yamazaki et al.* That is, *Yamazaki et al.* do not disclose or suggest a semiconductor thin film which corresponds to Applicant's claimed first semiconductor thin film, but instead only discloses a thin film connecting one transistor and another transistor, both of which are formed on the same surface of the substrate and utilizing the same process. Therefore, it is respectfully submitted that it would not have been obvious to one skilled in the art to combine the teachings of *Norman et al.* with those of *Yamazaki et al.* As such, since neither *Norman et al.* nor *Yamazaki et al.* disclose or suggest Applicant's claimed invention, nor the problems and objects associated therewith, it is submitted that Applicant's independent claim 1, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited references. It is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner's Action has also rejected claims 1 and 23-27 as being obvious over *Koga et al.* (USP 6,825,867) in view of *Yamazaki et al.* It is

submitted that these claims are *prima facie* patentably distinguishable over the cited references for at least the following reasons.

Koga et al. is directed to an organic electro-luminescent array exposure head. The exposure head 1, as shown in Figure 2, includes an organic light emitting part 4 disposed within a hole 8 formed within a partition wall 9. A light-emitting layer 10 is disposed at the base of the hole 8 and over a substrate 6. This reference also discloses forming TFTs 5 over the substrate 6. However, this reference does not disclose or suggest a first thin semiconductor film which includes at least a semiconductor device, and a second thin semiconductor film, which includes an integrated circuit, and both of which are formed on the same surface of a substrate as required by claim 1. The light-emitting layer 10 is not a thin semiconductor film, nor does it include a semiconductor device or an integrated circuit.

The Examiner's Action thus relies also on the teachings of *Yamazaki et al.* However, *Yamazaki et al.* do not overcome the above-noted deficiencies of *Koga et al.*, as pointed out above with respect to the rejection that utilized *Norman et al.* As such, it is submitted that the Examiner's Action has failed to provide a *prima facie* case of obviousness, and it is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner's Action has also rejected claims 28-31 as being obvious over *Sakai et al.* (USP 6,633,322) in view of *Yamazaki et al.* It is submitted that

these claims are *prima facie* patentably distinguishable over the cited combination of references for at least the following reasons.

The Examiner's Action admits that *Sasaki et al.* fail to disclose a thin semiconductor film. *Sakai et al.* disclose features similar to *Norman et al.* Moreover, this reference does not disclose or suggest that the first and second thin semiconductor films are less than or equal to 10 micrometers.

In accordance with Applicant's claim 28, since the semiconductor thin films are equal to or less than 10 micrometers thick, there is less possibility of a disconnection occurring between the interconnecting layer at a step of the semiconductor thin films, even if a tapered portion is not provided, such as shown by *Sakai et al.* Therefore, the invention of claim 28 has an increased reliability.

The Examiner's Action also relies on the teachings of *Yamazaki et al.* However, this reference does not overcome the deficiencies of *Sakai et al.*, and does not disclose or suggest Applicant's claimed first thin semiconductor film. Although this reference does disclose a transistor, which is shown in Figure 3B and is shown as a component below the orientation film 301 in Figure 6, this transistor is for driving a liquid crystal display device, which is shown as a liquid crystal material 308 in Figure 6, which is disposed separate from the transistor. However, the liquid crystal display device is not formed as a semiconductor thin film, and is not formed on the same surface of the substrate as the semiconductor thin film, so that this reference does not overcome the above-noted deficiencies of

Sakai et al. Further, *Yamazaki et al.* disclose a wiring layer which connects one transistor circuit and another transistor circuit, both of which are disposed on the same surface. However, since an element other than the transistor circuit, which is disposed on the same surface as the transistor circuit, is not disclosed by *Yamazaki et al.*, there is no disclosure or suggestion from this reference of connecting a transistor circuit with a light-emitting element (or a display element), both of which would be disposed on the same surface of the substrate, as would be required by Applicant's independent claim 28.

Moreover, since *Sakai et al.* disclose substantially the same invention as *Norman et al.*, similar to *Norman et al.*, there would have been no motivation to replace the second semiconductor thin film disclosed by *Sakai et al.* with a transistor as disclosed by *Yamazaki et al.*

As such, it is submitted that Applicant's claim 28, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited references. It is requested that these claims be allowed and that these rejections be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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